WHAT IS CLAIMED IS:

1. A synchronized output speech synthesizer, comprising:

a first memory for storing speech data;

a speech synchronizer for receiving the speech data stored by the first memory, thereby creating a speech signal output;

a second memory for storing signal data; and

a latch device for receiving the signal data stored by the second memory and thereby outputting a status signal;

wherein the speech synthesizer reading speech data of the first memory while, the latch device simultaneously reading the signal data of the second memory, and the speech synthesizer and the latch device outputting the voice and status signals in synchrony.

2. The synchronized output speech synthesizer device as defined in claim 1, further comprises a speaker for receiving the speech signal outputted by the speech synchronizer and playing the voice;

3. A synchronized output speech synthesizer device, comprising:

a first memory for storing speech data;

a speech synthesizer for receiving the speech data stored by the first memory, thereby creating a speech signal output;

a second memory for storing signal data; and

a multiplexer for receiving the signal data stored by the second memory and outputting a speech signal based on a selective signal received by a selective input ends; and

a latch device circuit for receiving the signal data output by the multiplexer, and

outputting a status signal;

wherein the speech synthesizer reading the speech data of the first memory , while the multiplexer simultaneously reading the signal data of the second memory through the latch device, and speech synthesizer and the latch device outputting the voice and status signals in synchrony.

4. The synchronized output speech synthesizer device as defined in claim 3, further comprises a speaker for receiving the speech signal outputted by the speech synchronizer and playing the voice.

5. The synchronized output speech synthesizer device as defined in claim 4, wherein the material received by the multiplexer includes the signal data, an output register data and a power-on reset signal.